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HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528			EXAMINER WHITMORE, STACY	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHRISTOPHER A. POIRIER, SAMUEL D. NAFFZIGER, and
CHRISTOPHER J. BOSTAK

Appeal 2009-007804
Application 10/644,625
Technology Center 2800

Before JOSEPH F. RUGGIERO, ROBERT E. NAPPI, and BRADLEY W.
BAUMEISTER, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL¹

¹ The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” (paper delivery mode) or the “NOTIFICATION DATE” (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Final Rejection of claims 1-32. At pages 11-13 of the Answer, the Examiner indicates that the rejections of claims 4, 5, 14, 15, 22, and 23 have been withdrawn. Accordingly, only the Examiner's rejection of claims 1-3, 6-13, 16-21, 24-27, and 29-32 is before us on appeal. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Appeal Brief (filed February 14, 2007), the Examiner's Answer (mailed May 18, 2007), and the Reply Brief (filed July 17, 2007).

Appellants' Invention

The invention claimed on appeal relates to the monitoring and controlling of an integrated circuit by an embedded microcontroller constructed on the same VLSI die as the integrated circuit. More particularly, the embedded microcontroller monitors temperatures at plural locations on the integrated circuit. (*See generally* Spec. ¶¶ [0013] and [0018-[0021]).

Claim 1 is illustrative of the invention and is reproduced as follows:

1. A system comprising:
an integrated circuit on a VLSI die; and
an embedded micro-controller constructed on the VLSI die, the micro-controller adapted to monitor and control the VLSI environment to optimize the integrated circuit operation;
wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit.

The Examiner's Rejection

The Examiner relies on the following prior art reference to show unpatentability:

Shakkarwar	US 6,694,492	Feb. 17, 2004 (filed Mar. 31, 2000)
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Claims 1-3, 6-13, 16-21, and 24-27 stand rejected under 35 U.S.C. 102(e) as being anticipated by Shakkarwar.²

ANALYSIS

Appellants' arguments focus on the contention that, in contrast to the requirements of each of the appealed independent claims 1, 8, 16, and 24, Shakkarwar provides no teaching or suggestion of monitoring temperatures at a "plurality of locations" on an integrated circuit. According to Appellants, while Shakkawar discloses that thermal parameters of an integrated circuit can be monitored, the monitoring of such thermal parameters is disclosed as occurring at only a *single* location, i.e., at the location of the single thermal sensor 107 (Fig. 1; col. 4, ll. 21-29 and col. 6, ll. 21-24).

We agree with Appellants. The Examiner makes reference (Ans. 3 and 5-7) to the portions of the disclosure of Shakkawar which describe the thermal parameter monitoring of an integrated circuit by applying test vectors to various sub-components of the integrated circuit and assessing the integrated circuit response to the test vectors (col. 4, ll. 16-54 and col. 6, ll.

² The Examiner has inadvertently omitted claims 6 and 7, which are discussed at pages 8 and 9 of the Answer, from the listing of claims included in this rejection. In addition, the Examiner has withdrawn the 35 U.S.C. § 103(a) rejection of claims 4, 5, 14, 15, 22, and 23.

39-52). As recognized by Appellants, Shakkawar does indeed disclose that thermal parameter monitoring of the integrated circuit may provide an indication as to how the integrated circuit is responding to test vectors applied to sub-components at different locations on the integrated circuit. As argued by Appellants (App. Br. 7; Reply Br. 3-4), however, the temperature monitoring in Shakkawar is taking place at only a single location, i.e., at the location of the thermal sensor 107, and not at a plurality of locations as claimed.

In view of the above discussion, we do not sustain the Examiner's 35 U.S.C. § 102(e) rejection of appealed independent claims 1, 8, 16, and 24, nor of claims 2, 3, 6, 7, 9-13, 17-21, 25-27, and 29-32 dependent thereon.

CONCLUSION

Based on the analysis above, we conclude that the Examiner erred in rejecting claims 1-3, 6-13, 16-21, 24-27, and 29-32 for anticipation under 35 U.S.C. § 102(e).

DECISION

The Examiner's decision rejecting claims 1-3, 6-13, 16-21, 24-27, and 29-32 under 35 U.S.C. § 102(e) is reversed.

Appeal 2009-007804
Application 10/644,625

REVERSED

ELD

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